[0060] What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A vertical MOS transistor comprising:

a semiconductor substrate;

a relaxed silicon germanium region formed over said substrate, said relaxed silicon germanium region having a graded germanium content;

source and drain regions disposed on opposite sides of said relaxed silicon germanium region; and

a strained silicon layer in contact with said relaxed silicon germanium region.

2. The vertical MOS transistor of claim 1 further comprising a silicon oxide layer in contact with said strained silicon layer.

3. The vertical MOS transistor of claim 2 further comprising a vertical transistor gate in contact with said silicon oxide layer.

4. The vertical MOS transistor of claim 3, wherein said vertical transistor gate is a polysilicon gate.

5. The vertical MOS transistor of claim 1, wherein said relaxed silicon germanium layer has a thickness of about 2,000 Angstroms to about 40,000 Angstroms between said source and drain regions.

6. The vertical MOS transistor of claim 1, wherein said relaxed silicon germanium layer is an epitaxially grown layer.

7. The vertical MOS transistor of claim 1, wherein said relaxed silicon germanium layer has a graded germanium content of about 0% to about 20%.

8. The vertical MOS transistor of claim 1, wherein said strained silicon layer has a thickness of about 200 Angstroms to about 2,000 Angstroms.

9. The vertical MOS transistor of claim 1, wherein said source and drain layer is an n+ silicon layer and said vertical MOS transistor is an NMOS transistor.

10. The vertical MOS transistor of claim 1, wherein said strained silicon layer is under a biaxial tensile strain.

11. The vertical MOS transistor of claim 1, wherein said semiconductor substrate is a silicon substrate.

12. An ultra-thin vertical NMOS transistor comprising:

a silicon substrate;

a relaxed silicon germanium region formed over said silicon substrate, said relaxed silicon germanium region having a graded germanium content from about 0% to about 20%;

source and drain regions disposed adjacent and on opposite sides of said relaxed silicon germanium region; and

a strained silicon layer in contact with said relaxed silicon germanium region with graded germanium content.

13. The ultra-thin vertical NMOS transistor of claim 12 further comprising a silicon oxide layer in contact with said strained silicon layer.

14. The ultra-thin vertical NMOS transistor of claim 13 further comprising a vertical polysilicon gate in contact with said silicon oxide layer.

15. The ultra-thin vertical NMOS transistor of claim 12, wherein said relaxed silicon germanium layer is an epitaxially grown layer by ultra high vacuum chemical vapor deposition.

16. The ultra-thin vertical NMOS transistor of claim 12, wherein said strained silicon layer is under a biaxial tensile strain.

17. A pseudo-NMOS output prediction logic circuit comprising:

a plurality of logic inputs, a clock input and an output, wherein each of said plurality of logic inputs is coupled to a plurality of gates of ultra-thin vertical NMOS transistors comprising a relaxed silicon germanium region with a graded germanium content of about 15% to about 20% and a strained silicon channel in contact with said relaxed silicon germanium region, and wherein the clock output is coupled to a gate of a vertical PMOS transistor for precharging the output high.

18. A dynamic output prediction logic circuit comprising:

a plurality of logic inputs, a clock input and an output, wherein each of said plurality of logic inputs is coupled to a plurality of gates of ultra-thin vertical NMOS transistors comprising a relaxed silicon germanium region with a graded germanium content of about 15% to about 20% and a strained silicon channel in contact with said relaxed silicon germanium region, and wherein the clock output is coupled to a gate of a vertical PMOS transistor for precharging the output high.

19. A processor-based system comprising:

a processor; and

an integrated circuit coupled to said processor, at least one of said integrated circuit and said processor comprising an ultra-thin vertical NMOS transistor including a relaxed silicon germanium body region with a graded germanium content of about 15% to about 20%; a strained silicon layer in contact with said relaxed silicon germanium body region; and source and drain regions formed adjacent said relaxed silicon germanium body region with said graded germanium content.

20. A method of forming a transistor comprising:

forming a first source/drain layer over a surface of a semiconductor substrate;

forming a relaxed silicon germanium layer over said first source/drain layer;

forming a second source/drain layer over said relaxed silicon germanium layer;

etching said first source/drain layer, said relaxed silicon germanium layer and said second source/drain layer to form at least one pillar extending outwardly from said surface of said semiconductor substrate;

forming a strained silicon layer on each sidewall of said at least one pillar;

forming an oxide layer over said strained silicon layer on one sidewall of said at least one pillar; and

forming a polysilicon layer on the sidewall opposite said one sidewall on which said oxide layer is formed.

21. The method of claim 20, wherein said relaxed silicon germanium layer is epitaxially grown by ultra high vacuum chemical vapor deposition.

22. The method of claim 20, wherein said relaxed silicon germanium layer is epitaxially grown by ultra high vacuum chemical vapor deposition using dichlorosilane and germane as precursors.

23. The method of claim 20, wherein the germanium content of said relaxed silicon germanium layer is further graded in steps.

24. The method of claim 23, wherein the germanium content of said relaxed silicon germanium layer is further graded in steps using a linear graded buffer technique.

25. The method of claim 24, wherein the germanium content of said relaxed silicon germanium layer is further graded in steps using a linear graded buffer technique by increasing the germanium content from 0 to about 20%.

26. The method of claim 20, wherein said relaxed silicon germanium layer is formed to a thickness of about 2,000 Angstroms to about 40,000 Angstroms.

27. The method of claim 20, wherein said strained silicon layer is epitaxially grown by ultra high vacuum chemical vapor deposition

28. The method of claim 20, wherein said strained silicon layer is formed to a thickness of about 200 Angstroms to about 2,000 Angstroms.

29. The method of claim 20, wherein said strained silicon layer formed in contact with said relaxed silicon germanium layer forms a biaxial tensile strain.

30. The method of claim 20, wherein said biaxial tensile strain modifies the band structure of said strained silicon layer.

31. The method of claim 20, wherein said biaxial tensile strain enhances the carrier transport in said strained silicon layer.

32. A method of forming a transistor structure, said method comprising:

providing at least one silicon germanium vertical pillar extending outwardly from a surface of a semiconductor substrate, said silicon germanium vertical pillar comprising a first source/drain layer formed over said semiconductor substrate, a relaxed silicon germanium layer formed over said first source/drain layer and a second source/drain layer formed over said relaxed silicon germanium layer; and

forming a strained silicon layer in contact with said at least one silicon germanium vertical pillar.

33. The method of claim 32, wherein said relaxed silicon germanium layer is epitaxially grown by ultra high vacuum chemical vapor deposition.

34. The method of claim 33, wherein said relaxed silicon germanium layer is epitaxially grown by ultra high vacuum chemical vapor deposition using dichlorosilane and germane as precursors.

35. The method of claim 32, wherein the germanium content of said relaxed silicon germanium layer is graded using a linear graded buffer technique.

36. The method of claim 35, wherein the germanium content of said relaxed silicon germanium layer is graded using a linear graded buffer technique to increase the germanium content from 0 to about 20%.

37. The method of claim 32, wherein said strained silicon layer is epitaxially grown by ultra high vacuum chemical vapor deposition